



# **basic education**

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Department:  
Basic Education  
**REPUBLIC OF SOUTH AFRICA**

## **ELECTRICAL TECHNOLOGY (DIGITAL ELECTRONICS)**

### **GUIDELINES FOR PRACTICAL ASSESSMENT TASKS (PAT)**

**GRADE 12**

**2023**

**These guidelines consist of 47 pages.**

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## 1. INTRODUCTION

The 18 Curriculum and Assessment Policy Statements subjects which contain a practical component all include a practical assessment task (PAT). These subjects are:

- **AGRICULTURE:** Agricultural Management Practices, Agricultural Technology
- **ARTS:** Dance Studies, Design, Dramatic Arts, Music, Visual Arts
- **SCIENCES:** Computer Applications Technology, Information Technology, Technical Sciences; Technical Mathematics
- **SERVICES:** Consumer Studies, Hospitality Studies, Tourism
- **TECHNOLOGY:** Civil Technology, Electrical Technology, Mechanical Technology and Engineering Graphics and Design

A practical assessment task (PAT) mark is a compulsory component of the final promotion mark for all candidates offering subjects that have a practical component and counts 25% (100 marks) of the end-of-the-year examination mark. The PAT is implemented across the first three terms of the school year. This is broken down into different phases or a series of smaller activities that make up the PAT. The PAT allows for learners to be assessed on a regular basis during the school year and it also allows for the assessment of skills that cannot be assessed in a written format, e.g. test or examination. It is therefore important that schools ensure that all learners complete the practical assessment tasks within the stipulated period to ensure that learners are resulted at the end of the school year. The planning and execution of the PAT differs from subject to subject.

Practical assessment tasks are designed to develop and demonstrate a learner's ability to integrate a variety of skills in order to solve a problem. The PAT also makes use of a technological process to inform the learner what steps needs to be followed to derive a solution for the problem.

The PAT consists of four simulations and a practical project. The teacher may choose any ONE of the practical projects and any TWO simulations available for DIGITAL ELECTRONICS.

The teacher must apply assessment on an ongoing basis at the same time that the learner is developing the required skills. TWO simulations should be completed by the learners, in addition to the manufacturing of a practical project.

The PAT incorporates all the skills the learner has developed throughout the year. The PAT ensures that all the different skills will be acquired by learners on completion of practical work, as well as the correct use of tools and instruments.

**Requirements for presentation**

A learner must present the following:

- PAT file with all the evidence of simulations, design and prototyping. A copy of the PAT 2023 cover page. The relevant simulations and assessment sheets should be copied and handed to each learner to include in the file.
- Practical project with:
  - Enclosure:
    - The file must include a design.
    - The enclosure and the design must match.
    - No cardboard boxes are allowed.
    - Plastic wooden and metal enclosures are acceptable.
    - Enclosures that are manufactured and/or assembled by the learners are preferred.
    - The enclosure should be accessible for scrutiny inside.
    - Lids that are secured are preferred.
  - Circuit board:
    - The file should include the PCB design.
    - The PCB must be mounted inside the enclosure in such a manner that it can be removed for scrutiny. Alternatively, inspection can be made from the bottom in cases where translucent (see-through) enclosures are used.
    - Switches, potentiometers, connectors and other items must be mounted.
    - Wiring must be neat and bound/wrapped.
    - Wiring must be long enough to allow for the PCB to be removed and inspected with ease.
  - Logo and name:
    - The file should contain the logo and name design and specification plate.
    - Logo, specification plate and name must be prominent on the enclosure.
    - The logo/specification plate must be affixed in a permanent manner – painted, glued or stuck on with vinyl.

The PAT will have a financial impact on the school's budget and school management teams are required to make provision to accommodate this particular expense.

PAT components and other items must be acquired timeously, for use by the learners, before the end of the first term at the start of the academic year.

It is the responsibility of the HOD to ensure that the teacher is progressing with the PAT from the start of the school year.

Provincial departments are responsible for setting up moderation timetables and consequently PATs should be completed in time for moderation.

## **2. TEACHER GUIDELINES**

### **2.1 How to administer PATs**

Teachers must ensure that learners complete the simulations required for each term. The project should be started in January in order to ensure its completion by August. In instances where formal assessments take place, the teacher has to assume the responsibility thereof.

The PAT should be completed during the FIRST THREE TERMS and must be ready at the start of PAT moderation. Teachers must make copies of the relevant simulations and hand them to learners at the beginning of each term.

**The PAT must NOT be allowed to leave the workshop and must be kept in a safe place at all times when learners are not working on them.**

The weightings of the PAT must be adhered to and teachers are not allowed to change weightings for the different sections.

### **2.2 How to mark/assess the PATs**

The PAT for Grade 12 will be set and assessed internally, but moderated externally. All formal assessment will be done by the teacher.

The teacher is required to produce a working model and model answer file that sets the baseline for assessment at a Highly Competent Level for every project choice exercised by the learners. This file must include all the simulations with answers the teacher has done him/herself. The teacher will use the model answers and project to assess the simulations and projects of the learners.

Once a facet sheet has been completed by the teacher, assessment will be deemed to be complete. No re-assessment will be done once the facet sheets have been completed and captured by the teacher. Learners must ensure that the work is done to the required standard before the teacher finally assesses the PAT during each stage of completion.

**2.3 PAT Programme of Assessment (PAT PoA)**

The programme of assessment (PoA) of the PAT is as follows:

TIME FRAME	ACTIVITY	RESPONSIBILITY
	Preparation for PAT 2023	Teacher – Builds the models and works out the model answers for the simulations. Identifies shortages in tools, equipment and consumable items for simulations that must be procured. SMT – Receives procurement requests from teachers and processes payments for the acquisition of required items
January–March 2023	Simulation 1	Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations HOD – Checks if tasks have been completed and marked by the teacher before the holidays
January 2023	PAT project – procurement	Teacher – Obtains quotations for PAT projects Principal – Approves PAT procurement for PAT projects Teacher – Ensures that PAT projects are ordered and delivered HOD – Checks in on teacher to see if the process is adhered to
February 2023	PAT project – learners commence with project	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Includes practical sessions for learners to complete the PAT project every week Learners – Commence with completion of the PAT project HOD – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis
April–June 2023	Simulation 2	Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations HOD – Checks if tasks have been completed and marked by the teacher before the holidays
April–June 2023	Moderation of Simulation 1	District subject facilitator/subject specialist will visit the school and moderate Simulation 1 10% of learners' work is moderated
April–June 2023	PAT project – learners continue with project	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Includes practical sessions every week for learners to complete the PAT project Learners – Continue with completion of the PAT project HOD – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis
July holidays 2023	PAT intervention	Learners that are behind on the PAT are required to complete the project during these holidays.
July–August 2023	Moderation of Simulation 2	District subject facilitator/subject specialist will visit the school and moderate Simulation 2 – different learners from the previous term 10% of learners' work is moderated
July–August 2023	PAT project – completion	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Completes the PAT project with learners and compiles the PAT file Learners – Complete the PAT project and file HOD – Checks to see that 100% of the PAT files and projects are completed and assessed
September–October 2023	PAT moderation	PAT projects are moderated by subject facilitators/subject specialists from the province and learners are available to demonstrate skills 10% of learners are moderated randomly

## 2.4 Moderation of PATs

Provincial moderation of each term's simulations will start as early as the following term. Simulation 1 should be moderated as soon as the second term starts. Similarly, Simulation 2 will be moderated in July. The project will, however, only be moderated on completion.

During moderation of the PAT, the learner's file and project must be presented to the moderator.

The moderation process is as follows:

- During moderation, learners are randomly selected to demonstrate the different simulations. All four simulations will be moderated.
- The teacher is required to build an exemplar model of each project type chosen for the school.
- This model must be on display during moderation.
- The teacher's model forms the standard of the moderation at Level 4 (Highly Competent).
- Level 5 assessments must exceed the model of the teacher in skill and finishing.
- Learners who are moderated will have access to their files during moderation and may refer to the simulations they completed earlier in the year.
- Learners may NOT ask assistance from other learners during moderation.
- All projects and files must be on display for the moderator.
- If a learner is unable to repeat the simulation or cannot produce a working circuit during moderation, marks will be deducted and circuits assessed as not being operational.
- The moderator will randomly select no fewer than two projects (not simulations) and the learners involved will have to explain how the project was manufactured.
- Where required, the moderator should be able to call on the learner to explain the function and principles of operation, and request the learner to exhibit the skills acquired through the simulations for moderation purposes.
- On completion the moderator will, if needed, adjust the marks of the group upwards or downwards, depending on the outcome of moderation.
- Normal examination protocols for appeals will be adhered to, if a dispute arises from adjustments made.

## 2.5 Absence/Non-submission of tasks

The absence of a PAT mark in Electrical Technology without a valid reason: The learner will be given three weeks before the commencement of the final end-of-year examination to submit the outstanding task. Should the learner fail to fulfil the outstanding PAT requirement, such a learner will be awarded a zero (0) for that PAT component.

## 2.6 Simulations

Simulations are circuits, experiments and tests/tasks which the learner will have to build, test and measure and practically do as part of the development of practical skills. These skills have to be illustrated to the external moderator that visits the school at intervals during the school year.

Teachers who make use of simulation programs on a computer may use them for the learners to practise on. However, it is required that the circuit be built using real components and that measurements be made with actual instruments for the purposes of assessment and moderation.

The correct procedure for completing simulations is outlined below for teachers and school management teams who are responsible for the implementation of the PAT in Electrical Technology.

- STEP 1: The teacher will choose simulations from simulations that are provided.
- STEP 2: Compile a list of the components needed for every simulation. Add extra components as these items are very small and you will need extras, as these items get lost/damaged very easily when learners work on them.
- STEP 3: Contact three different electronics component suppliers for comparative quotations.
- STEP 4: Submit the quotations to the SMT for approval and procurement of the items.
- STEP 5: Place the components in storage. Collate items for each simulation, thus making it easier to distribute and use during practical sessions. Ensure that different values of components do not mix, as this would lead to components being used incorrectly and this could damage the component and in extreme cases, the equipment used.
- STEP 6: Copy the relevant simulations and hand them out to learners at the start of the term.

Teachers are allowed to adjust circuits and component values to suit their environment/resource availability.

Teachers are required to develop a set of model answers in the teacher's file. Moderators will use the teacher's model answers and artefacts when moderating.

## 2.7 Projects

The projects are construction projects teachers can choose for their learners. These projects are based on proven circuits provided by schools and subject advisors. The projects are based on working prototypes and require careful construction in order for it to operate correctly.

Projects vary in cost and teachers must ensure that the projects chosen fall within the scope of the school's budget.

Once the teacher has decided on a circuit, he/she must construct the prototype. Thereafter, copies of the provided circuit can be made and distributed to learners. They **MUST** redraw these circuits in their files correctly.

The description of the operation of the circuits is **NOT** complete. Learners are required to interrogate the function of the components in the provided circuit. Learners should elaborate on the purpose of components in the circuit. It is recommended that learners investigate similar circuits available on the internet and in the school library or workshop reference books.



**2.8 Working mark sheet**

(A working Excel file is provided with this PAT.)

PAT mark sheet		Term 1	Term 2	Project		Total = Term 1 + Term 2 + Project	Mark out of 100	Moderated Mark
No.	Name of Learner	Simulation 1	Simulation 2	Design and Make Part 1	Design and Make Part 2			
		50	50	120	30	250		
1.								
2.								
3.								
4.								
5.								
6.								
7.								
8.								
9.								
10.								
11.								
12.								
13.								
14.								
15.								
	<b>Total</b>							
	<b>Average</b>							

Teacher Name: \_\_\_\_\_

Principal Name: \_\_\_\_\_

Moderator Name: \_\_\_\_\_

Signature: \_\_\_\_\_

Signature: \_\_\_\_\_

Signature: \_\_\_\_\_

Date: \_\_\_\_\_

Date: \_\_\_\_\_

Date: \_\_\_\_\_

**3. LEARNER GUIDELINES****3.1 PAT 2023 COVER PAGE**

(Place this page at the front of the PAT.)

**Department of Basic Education Grade 12**  
**CAPS for Technical High Schools Practical Assessment Task – Electrical Technology**

Time allowed: Terms 1–3 (2023)

Learner Name: \_\_\_\_\_

Class: \_\_\_\_\_

School: \_\_\_\_\_

Specialisation: DIGITAL ELECTRONICS

Complete any **TWO** simulations.

Project (Write the name of the project): \_\_\_\_\_

Evidence of moderation:

**NOTE:**

When the learner evidence selected has been moderated at school level, the table will contain evidence of moderation. Provincial moderators will sign the provincial moderation and only sign if re-moderation is needed.

Moderation	Signature	Date	Signature	Date
School-based				
District moderation				
Provincial moderation			Re-moderation	

Mark allocation

PAT Component	Maximum Mark	Learner Mark	Moderated Mark
Simulation 1	50		
Simulation 2	50		
Design and Make Project – Circuit	120		
Design and Make Project – Enclosure	30		
<b>Total</b>	<b>250</b>		

### 3.2 Instructions to the learner

- The practical assessment task counts 25% of your final promotion mark.
- All work produced by you must be your own effort. Group work and co-operative work are NOT allowed.
- The practical assessment task must be completed over three terms.
- The PAT file must contain TWO simulations and a practical project.
- Calculations should be clear and include units. Calculations should be rounded off to TWO decimals. SI units should be used.
- Circuit diagrams can be hand-drawn or drawn on CAD. NO photocopies or scanned files are allowed.
- Photos are allowed and may be in colour or greyscale. Scanned photos and photocopies are allowed.
- This document must be placed inside your PAT file together with the other evidence.
- Learners with identical photos will be penalised and receive zero for that section.

### 3.3 Declaration of Authenticity (COMPULSORY)

Declaration:

I \_\_\_\_\_ (name) herewith declare that the work represented in this evidence is entirely my own effort. I understand that if proven otherwise, my final results may be withheld.

\_\_\_\_\_  
Signature of learner

\_\_\_\_\_  
Date

**4. SIMULATIONS****4.1 Simulation 1: Inverting op amp**

Name of learner: _____		Mark <div style="border: 1px solid black; padding: 5px; display: inline-block; width: 100px; text-align: center;">50</div>
Class: _____	Date completed: _____	
Date Assessed: _____	Assessor Signature: _____	
Date Moderated: _____	Moderator Signature: _____	

**Purpose:**

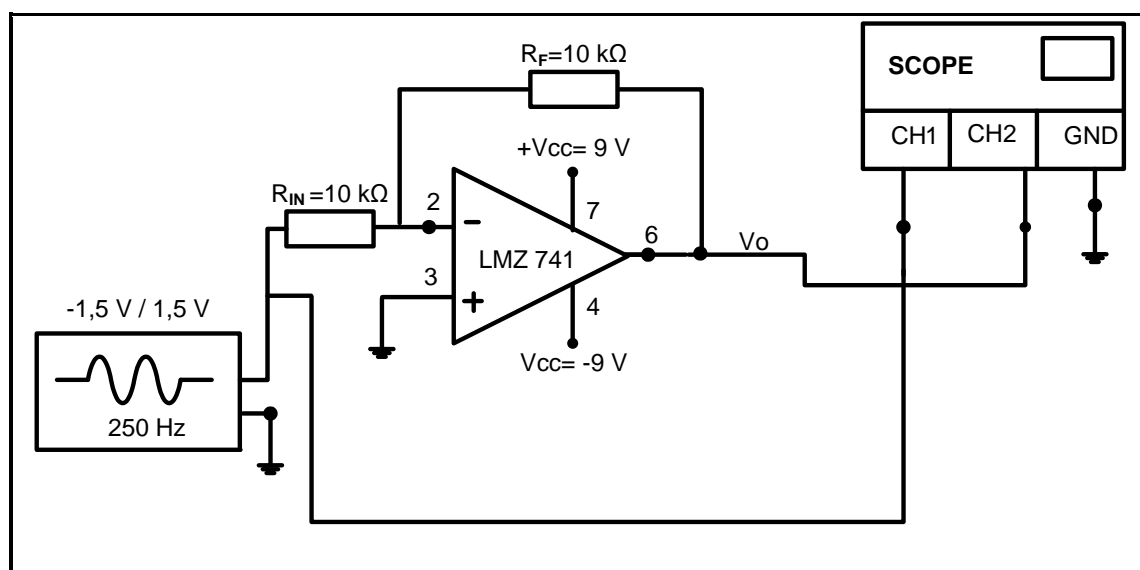
- To build an inverting operational amplifier circuit using a 741 op-amp integrated circuit (IC)
- To display the output waveforms on an oscilloscope
- To observe how a change in the value of  $R_F$  affects the gain and output voltage of the circuit

**Required resources:**

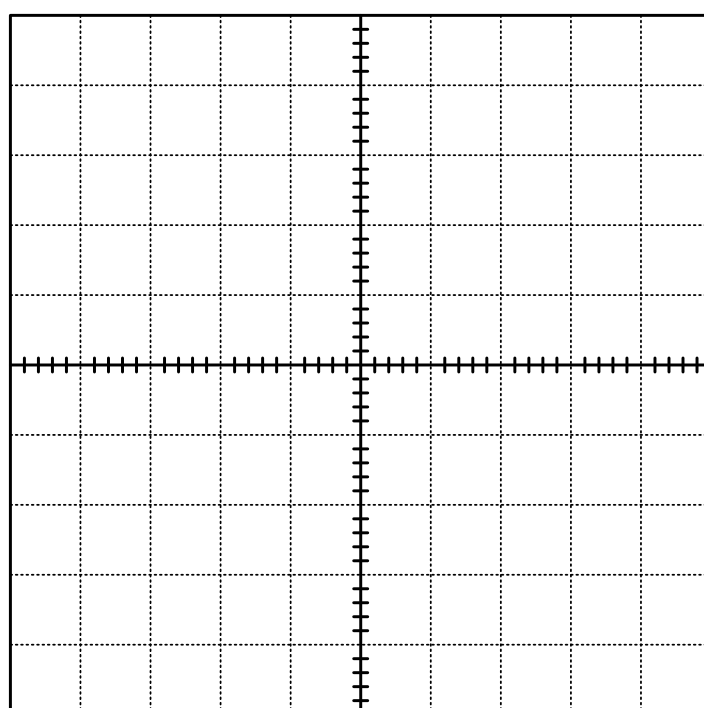
TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer Analogue/Digital oscilloscope (dual trace) Function generator Multimeter Variable DC power supply (split supply) Side cutters Wire stripper Long-nose pliers Breadboard	1 x LM 741 op amp 2 x 10 k $\Omega$ for $R_{IN}$ and $R_F$ 1 x 15 k $\Omega$ , 22 k $\Omega$ , 33 k $\Omega$ , 47 k $\Omega$ , 56 k $\Omega$ and 82 k $\Omega$ for $R_F$ Connecting wires

**Procedure:**

- 4.1.1 Construct the circuit on the breadboard as shown in FIGURE 4.1.1.

**FIGURE 4.1.1: INVERTING OP AMP**

- 4.1.2 Ensure CH1 and CH2 are set to 0,5 V/division. The time setting must be set on 1 ms/division.
- 4.1.3 Draw and label both the input (from CH1) and output (from CH2) waveforms for TWO complete cycles on the table below. (4)
- 4.1.4 Write down the peak values of the input and output voltage readings from CH1 and CH2 with  $R_F = 10 \text{ k}\Omega$ .



CH 1 V/div: 0,5 V

CH 2 V/div: 0,5 V

Time/div: 1 ms

 $V_{IN}$  : \_\_\_\_\_ $V_{OUT}$  : \_\_\_\_\_**TABLE 4.1.4****NOTE:** 2 marks for each correct waveform

(2)

- 4.1.5 Use the peak values in QUESTION 4.1.4 to calculate the gain below.  
(All values measured with the oscilloscope are peak values.)

$$A_V = - \left( \frac{V_{OUT(peak)}}{V_{IN(peak)}} \right)$$

= \_\_\_\_\_

= \_\_\_\_\_

(2)

- 4.1.6 Calculate the voltage gain of the circuit by using the formula below.

$$A_V = - \left( \frac{R_F}{R_{IN}} \right)$$

= \_\_\_\_\_

= \_\_\_\_\_

(2)

- 4.1.7 Measure and record the voltages across  $V_{OUT}$  in the table below. Also calculate the voltage gain values in the table below as you change the value of  $R_F$  in the circuit.  
Use  $A_V = - \left( \frac{V_{OUT}}{V_{IN}} \right)$

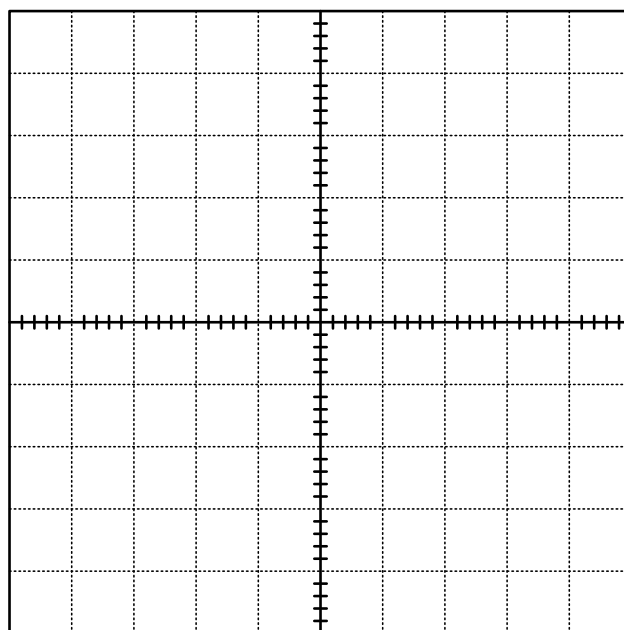
Resistor $R_F$	$V_{IN}$	$V_{OUT}$	Voltage gain ( $A_V$ )
(a) 22 k $\Omega$	1,5 V	_____	
(c) 47 k $\Omega$	1,5 V	_____	
(d) 100 k $\Omega$	1,5 V	_____	

TABLE: 4.1.7

**NOTE:** 1 mark for each correct voltage value = 3  
2 marks for each correct gain calculation = 6

(9)

- 4.1.8 Draw and label the input and output waveforms for at least two complete cycles in the table below. Indicate the voltage settings for CH1 and CH2 with  $R_F = 100 \text{ k}\Omega$ .



CH 1 V/div: \_\_\_\_\_

CH 2 V/div: \_\_\_\_\_

Time/div: 1 ms

**TABLE 4.1.8**

**NOTE:** 2 marks for each correct waveform  
1 mark for each voltage setting

(6)

- 4.1.9 Calculate the gain of the amplifier by using resistance values when  $R_F = 100 \text{ k}\Omega$ .

$$A_V = - \left( \frac{R_F}{R_{IN}} \right)$$

= \_\_\_\_\_

= \_\_\_\_\_

(2)

- 4.1.10 Refer to TABLE 4.1.7, your waveforms in TABLES 4.1.4 and 4.1.8 as well as your calculations in QUESTIONS 4.1.6 and 4.1.9. Compare the gain in QUESTION 4.1.6 to the gain in QUESTION 4.1.9 above and write a conclusion to your findings.

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(5)

**Theory Simulation 1:****[32]**

**NOTE: Learner competency in this context will mean the following:  
(This is done for easy assessment when using a rubric.)**

<b>Not yet competent</b>	Have not met the requirements and will be given another opportunity for reassessment. <ul style="list-style-type: none"><li>• Be precise about what they did wrong, or the areas they need to improve in.</li><li>• Explain clearly the level of skill they need to achieve to be assessed as 'competent'.</li><li>• Indicate whether part or all of the assessment event will need to be repeated.</li></ul>
<b>Competent</b>	Have the necessary ability, knowledge or skill to complete the task successfully. <ul style="list-style-type: none"><li>• Acceptable and satisfactory, though not outstanding.</li></ul>
<b>Outstanding</b>	Went beyond expectation (neatness, proficiency – high degree of skills, expertise)



## FACET SHEET FOR SIMULATION 1

Task description	Mark allocation (tick the appropriate level next to the task indicated)				Allocation of marks
	Competent after reassessment of certain parts of the task	Not yet competent after reassessment of certain/all parts of the task	Competent	Outstanding (Highly competent)	
<b>Building the inverting op amp using LM 741 IC</b>	The learner was given opportunities to rebuild the circuit after the teacher intervened in identifying and rectifying more mistakes.  (1–3)	The learner was given an opportunity to rebuild part of the circuit after the teacher intervened in identifying and rectifying a few mistakes.  (4–6)	The learner correctly built the circuit without the guidance of the teacher.  (7–9)	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency. (10–12)	<u>12</u>
<b>Safety aspects</b>	The learner was timeously reminded to apply safety rules, regulation and correct procedure when using tools and instruments.  (1)	The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments.  (2)	The learner applied safety rules, regulation and correct procedure when using tools and instruments to wire the circuits without being reminded by the teacher. (3)		<u>3</u>
<b>Attitude/ Behaviour/ Conduct</b>	The learner was reluctant to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice even after being cautioned/reprimanded.  (0)	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice.  (1–2)	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice.  (3)		<u>3</u>
<b>Rubric Theory</b> <b>Total Simulation 1</b>					<u>18</u> + <u>32</u> = <u>50</u>

**4.2 Simulation 2: Switching circuits using a 555 IC and a 741 op amp****Simulation 2A: Switching circuits using a 555 IC and a 741 op amp**

Name of learner: _____		Mark <div style="border: 1px solid black; width: 100px; height: 30px; margin: 0 auto; display: flex; align-items: center; justify-content: center;">50</div>
Class: _____	Date completed: _____	
Date Assessed: _____		Assessor Signature: _____
Date Moderated: _____		Moderator Signature: _____

**4.2.1 Purpose:**

- To build an electronic piano (astable multivibrator) circuit using a 555 IC in FIGURE 4.2.2 on a breadboard
- To display the output waveforms on an oscilloscope
- To calculate the output frequency
- To investigate how a change in  $R_{IN}$  affects the frequency and tone of the output

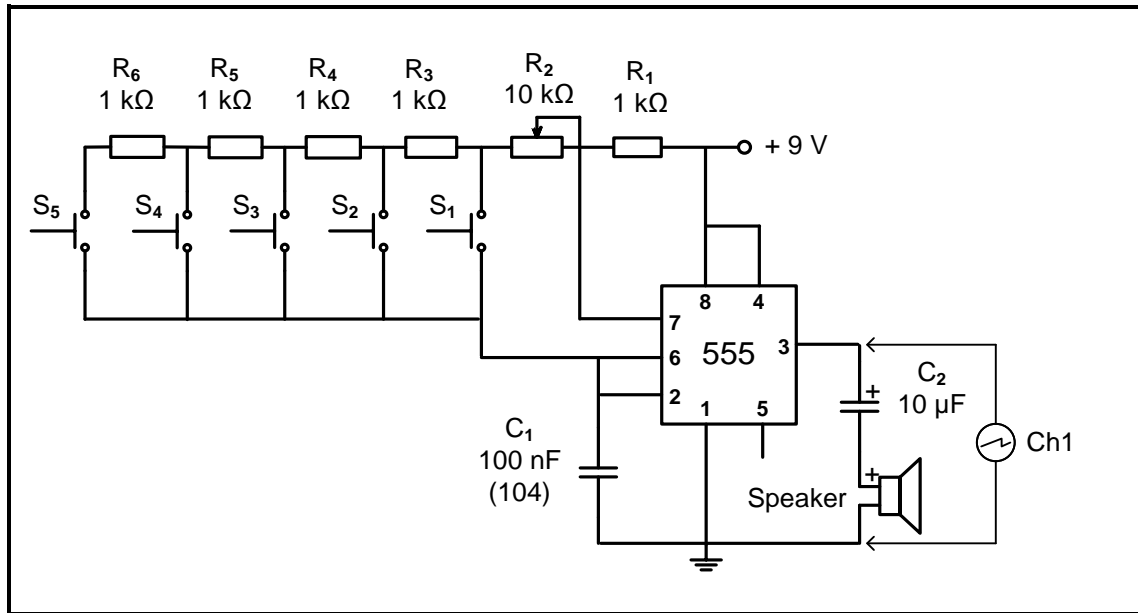
**4.2.2 Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer	1 x 555 IC
Analogue/Digital oscilloscope	1 x 100 nF capacitor
Variable DC power supply	1 x 10 $\mu$ F (electrolytic capacitor 25 V)
Side cutters	5 x 1 k $\Omega$ resistor
Wire stripper	1 x 10 k $\Omega$ potentiometer
Long-nose pliers	1 x 8 $\Omega$ speaker/buzzer
Breadboard	5 x push buttons
	Connecting wires

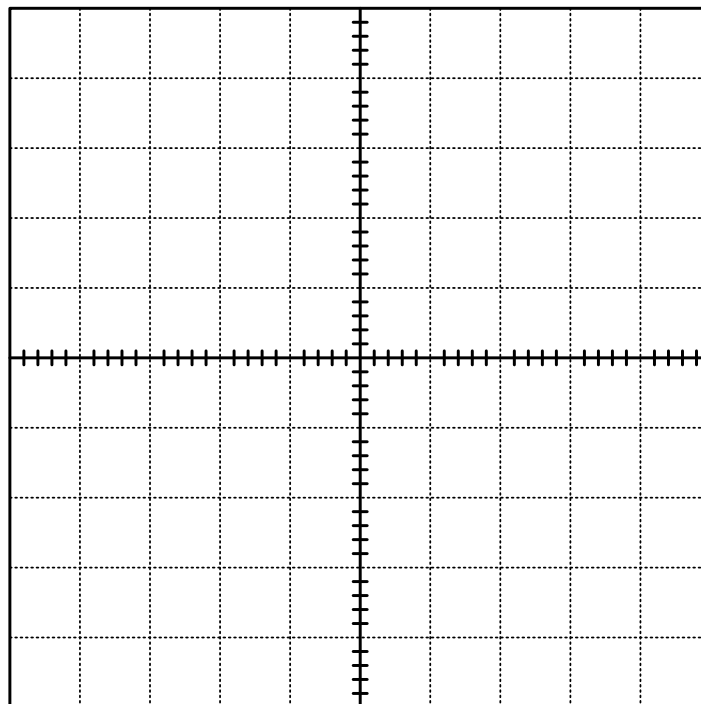
**4.2.3 Procedure:**

- (a) Build the circuit in FIGURE 4.2.3 on the breadboard.  
 Set the 10 k $\Omega$  POT to 6,5 k $\Omega$  before connecting it in the circuit.  
 Connect channel 1 of the oscilloscope to pin 3 of the 555 IC.  
 Switch the circuit ON, press the push buttons (one at a time) and observe.  
 Answer the questions that follow.

**NOTE:** If there is noise, pin 5 can be connected to ground via a capacitor of (0,01 $\mu$ F).

**FIGURE 4.2.3: ASTABLE MULTIVIBRATOR**

- (b) Press push button  $S_1$  and draw the output wave observed on the oscilloscope grid provided. Set the oscilloscope to display at least FOUR complete cycles.



CH 1 V/div: \_\_\_\_\_

Time/div: \_\_\_\_\_

**NOTE:** 1 mark for the correct waveform  
1 mark for the oscilloscope setting

(2)

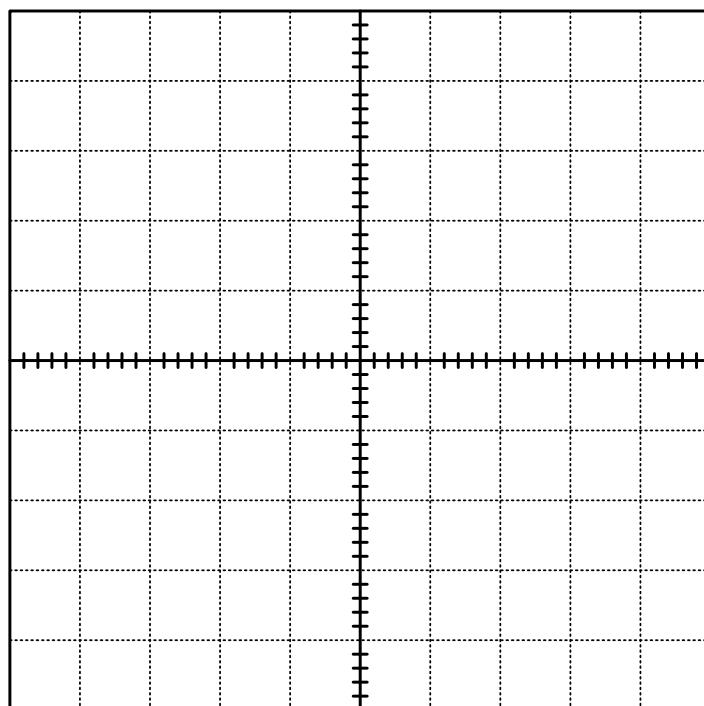
- (c) Use the oscilloscope settings and determine the frequency of the signal.

Frequency when  $S_1$  is pressed \_\_\_\_\_

\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

(2)

- (d) Press push button  $S_5$  and draw the output wave observed on the oscilloscope grid provided. Do not adjust the time per division setting.



CH 1 V/div: \_\_\_\_\_

Time/div: \_\_\_\_\_

**NOTE:** 1 mark for the correct waveform  
1 mark for the oscilloscope settings

(2)

- (e) Use the oscilloscope settings and determine the frequency of the signal.

Frequency when  $S_5$  is pressed

\_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

(2)

- (f) Press each of the push buttons and observe.

Explain why there is a difference in the output for each push button.

\_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

(2)

Theory Simulation 2A

[10]

## FACET SHEET FOR SIMULATION 2A

Task description	Mark allocation (tick the appropriate level next to the task indicated)				Allocation of marks
	Competent after reassessment of certain parts of the task	Not yet competent after reassessment of certain/all parts of the task	Competent	Outstanding (Highly competent)	
<b>Building the astable multivibrator using 555 IC</b>	The learner was given opportunities to rebuild the circuit after the teacher intervened in identifying and rectifying more mistakes.  (1–2)	The learner was given an opportunity to rebuild part of the circuit after the teacher intervened in identifying and rectifying a few mistakes.  (3–4)	The learner correctly built the circuit without the guidance of the teacher.  (5–6)	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency. (7–9)	$\overline{9}$
<b>Safety aspects</b>	The learner was timeously reminded to apply safety rules, regulation and correct procedure when using tools and instruments.  (1)	The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments.  (2)	The learner applied safety rules, regulation and correct procedure when using tools and instruments to wire the circuits without being reminded by the teacher. (3)		$\overline{3}$
<b>Attitude/ Behaviour/ Conduct</b>	The learner was reluctant to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice even after being cautioned/reprimanded. (0)	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. (1–2)	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. (3)		$\overline{3}$
<b>Rubric Theory</b> <b>Total Simulation 2A</b>					/15 + /10 = /25

**Simulation 2B: Schmitt trigger 741 IC****4.2.4 Purpose:**

- To build the Schmitt trigger circuit in FIGURE 4.2.6 using a 741 op amp and displaying the input and output waveforms on an oscilloscope
- To investigate the effect of the  $R_F$  to  $R_1$  ratio on the trigger voltage and output of the circuit

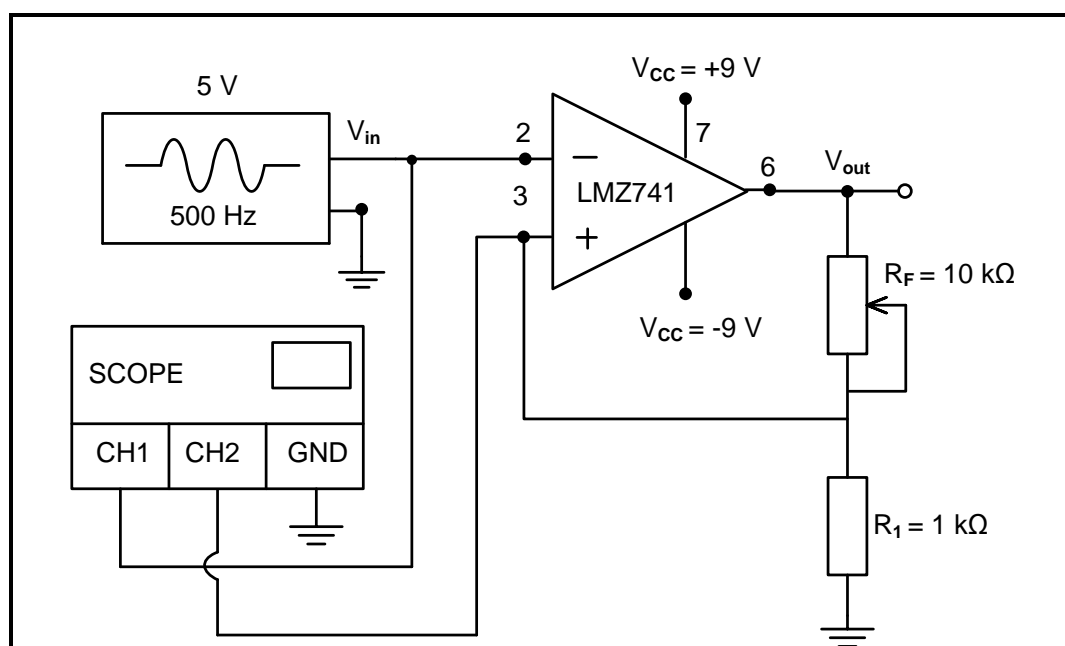
**4.2.5 Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Function generator	1 x LM741 op amp
Dual-trace oscilloscope	1 x 1 k $\Omega$ resistor
+9 V 0 V -9 V DC power supply	1 x 10 k $\Omega$ potentiometer
Side cutters	Connecting wires
Wire stripper	
Calculator	

**4.2.6 Procedure:**

- Set the dual voltage power supply to +9 V/-9 V.
- Set the function generator to deliver a 5 V peak 500 Hz sine wave.
- Build the circuit in FIGURE 4.2.6(a) on your experiment board and connect it to the supply and input.
- Connect channel 1 of the oscilloscope across the inverting input to display at least TWO complete cycles.
- Connect channel 2 of the oscilloscope across the non-inverting input to display at least TWO complete cycles.
- Ensure that the V/div settings for channel 1 and channel 2 are the same.
- Set the T/div setting to display at least TWO complete cycles of the input and output.
- After measuring the voltage on the non-inverting input, use channel 2 to display the output.

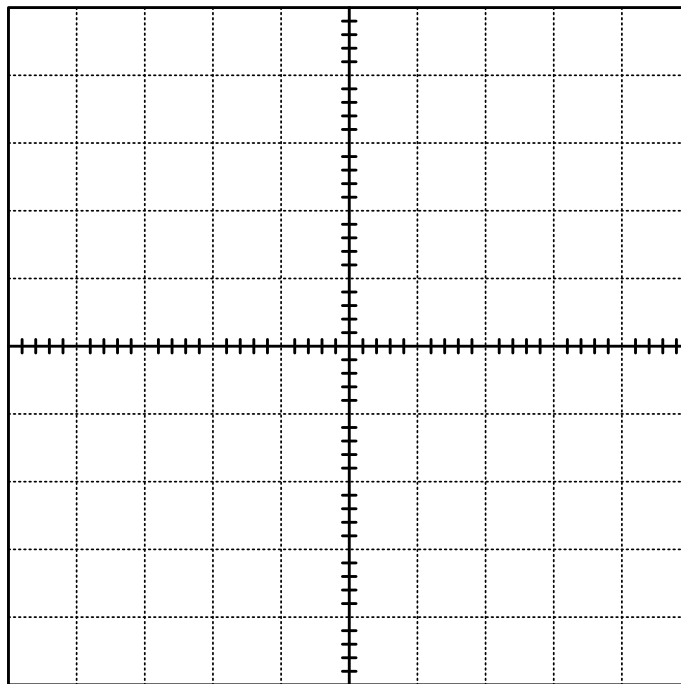
(a) Build the circuit in FIGURE 4.2.6(a) on the experiment board.



**FIGURE 4.2.6(a): 741 SCHMITT TRIGGER**

- (b) Draw and label the input waveforms from pin 2 and pin 3 on the oscilloscope grid below.

Keeping the V/div settings the same, change channel 2 connection from pin 3 to pin 6 (output) and draw and label the output waveform on the oscilloscope grid below.



CH 1 V/div: \_\_\_\_\_

CH 2 V/div: \_\_\_\_\_

Time/div: \_\_\_\_\_

**NOTE:** 1 mark for each correct waveform = 3  
1 mark for the oscilloscope settings

(4)

- (c) Set  $R_F$  resistor to the following values and complete TABLE 4.2.6(c) below.

$R_F$	Non-inverting voltage (pin 3)
8 k $\Omega$	
5 k $\Omega$	
2 k $\Omega$	

**TABLE 4.2.6(c)**

(3)

- (d) Refer to TABLE 4.2.6(c) above and your observation when changing the value of  $R_F$ . Write down a conclusion about the effect of the  $R_F$  to  $R_1$  ratio on the trigger voltage levels of the Schmitt trigger.

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(3)

## FACET SHEET FOR SIMULATION 2B

Task description	Mark allocation (tick the appropriate level next to the task indicated)				Allocation of marks
	Competent after reassessment of certain parts of the task	Not yet competent after reassessment of certain/all parts of the task	Competent	Outstanding (Highly competent)	
<b>Building the astable op amp using 555 IC</b>	The learner was given opportunities to rebuild the circuit after the teacher intervened in identifying and rectifying more mistakes.  (1–2)	The learner was given an opportunity to rebuild part of the circuit after the teacher intervened in identifying and rectifying a few mistakes.  (3–4)	The learner correctly built the circuit without the guidance of the teacher.  (5–6)	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency. (7–9)	<u>9</u>
<b>Safety aspects</b>	The learner was timeously reminded to apply safety rules, regulation and correct procedure when using tools and instruments.  (1)	The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments.  (2)	The learner applied safety rules, regulation and correct procedure when using tools and instruments to wire the circuits without being reminded by the teacher. (3)		<u>3</u>
<b>Attitude/ Behaviour/ Conduct</b>	The learner was reluctant to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice even after being cautioned/reprimanded.  (0)	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice.  (1–2)	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice.  (3)		<u>3</u>
					<b>Rubric Theory</b> /15
					<b>Total Simulation 2B</b> +      /10
					<b>Total Simulation 2A</b> =      /25
					<b>TOTAL:</b> +      /25
					<b>TOTAL:</b> =      /50



**4.3 Simulation 3: Connecting a 7-segment display to a 4-bit BCD 7-segment driver**

Name of learner: _____		Mark <div style="border: 1px solid black; width: 100px; height: 30px; margin: 0 auto; text-align: center; line-height: 30px;"><b>50</b></div>
Class: _____	Date completed: _____	
Date Assessed: _____		Assessor Signature: _____
Date Moderated: _____		Moderator Signature: _____

**4.3.1 Purpose:**

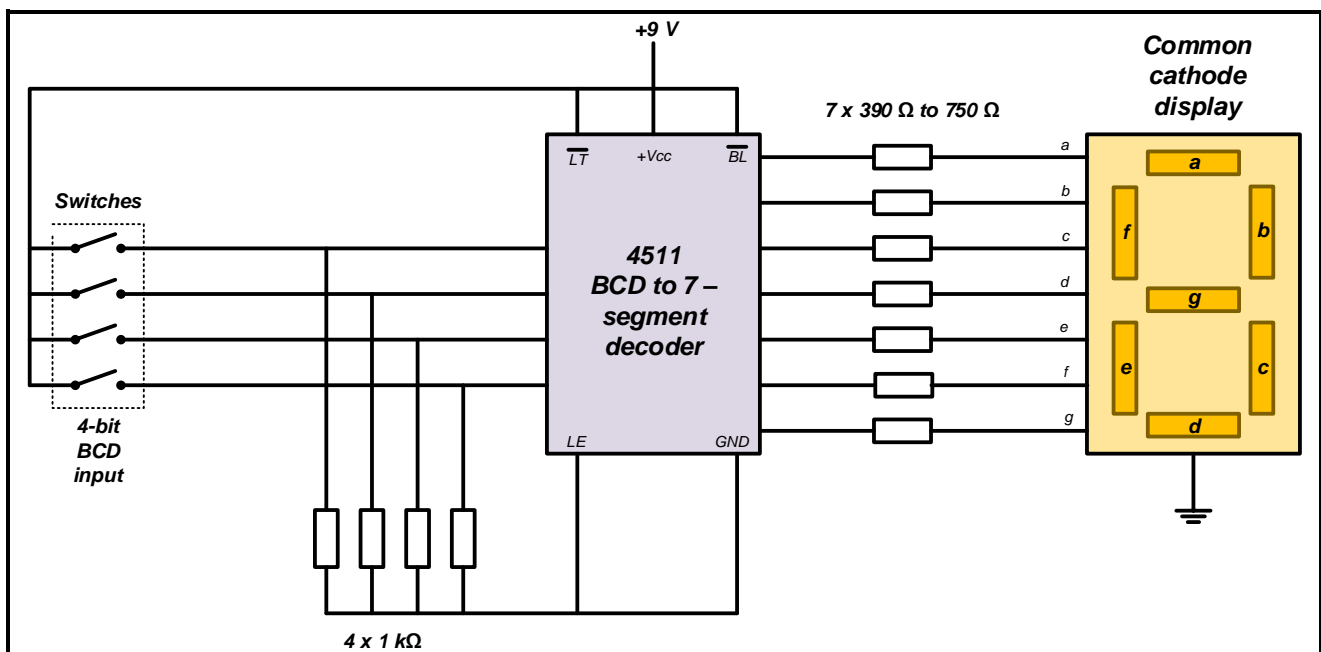
- To connect a 7-segment display to a 4-bit BCD 7-segment display driver

**4.3.2 Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer Breadboard Variable DC power supply Side cutters Breadboard wire	4 x LEDs 4 x 390 $\Omega$ resistors 7 x 1k resistors CD4511 IC CD4518B IC 5 x SPST switches 7-segment display

**4.3.3 Activity 3A**

Connect the circuit as in the circuit given below.



## FACET SHEET FOR SIMULATION 3

Task description	Mark allocation (tick the appropriate level next to the task indicated)				Allocation of marks
	Competent after reassessment of certain parts of the task	Not yet competent after reassessment of certain/all parts of the task	Competent	Outstanding (Highly competent)	
<b>Building the 7-segment display to a 4-bit BCD 7-segment display driver</b>	The learner was given opportunities to rebuild the circuit after the teacher intervened in identifying and rectifying more mistakes. (1)	The learner was given an opportunity to rebuild part of the circuit after the teacher intervened in identifying and rectifying a few mistakes. (2-3)	The learner correctly built the circuit without the guidance of the teacher. (4-5)	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency. (6)	<u>6</u>
<b>Safety aspects</b>	The learner was timeously reminded to apply safety rules, regulation and correct procedure when using tools and instruments. (1)	The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments. (2)	The learner applied safety rules, regulation and correct procedure when using tools and instruments to wire the circuits without being reminded by the teacher. (3)		<u>3</u>
<b>Hand tools</b>	Used hand tools correctly (1)				<u>1</u>
<b>Preparation for insertion of components into breadboard</b>	Checked the datasheet on the ICs (1)	Set supply voltage correct at +9 V (2)			<u>2</u>
<b>Correct connection on breadboard – nodes and polarity</b>	8 nodes for correct connection of CB4518B IC (8)	15 nodes for correct connection of CD4511 IC and the 7-segment display (15)	20 nodes for correct connection of CD4511 IC and the 7-segment display (20)		<u>20</u>
<b>Attitude/ Behaviour/ Conduct</b>	The learner was reluctant to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice even after being cautioned/ reprimanded. (0)	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. (1-2)	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. (3)		<u>3</u>
<b>Rubric</b>					<b>/35</b>

**Activity 3B**

Conduct the following steps and answer the questions in the spaces provided.

STEP	IC CD4185 GIVEN CODE	7-SEGMENT DISPLAY
(a)	Which number is displayed on the 7-segment display driver if the binary number 0111 is illuminated on the output LEDs of the counter?	
(b)	Which number is displayed on the 7-segment display driver if the binary number 1000 is illuminated on the output LEDs of the counter?	
(c)	Which number is displayed on the 7-segment display driver if the binary number 1001 is illuminated on the output LEDs of the counter?	
(d)	Explain what will happen to the output when only switches C and D are switched ON.	
(e)	Explain what will happen to the output when only switches B and D are switched ON.	

(3)

(3)

(3)

(3)

(3)

**[15]****Activity 3A: (35)****Activity 3B: (15)****TOTAL Simulation 3: [50]**

**4.4 Simulation 4: J-K flip-flop circuit and PICAXE**

Name of learner: _____		Mark <div style="border: 1px solid black; padding: 5px; text-align: center;"><b>50</b></div>
Class: _____	Date completed: _____	
Date Assessed: _____	Assessor Signature: _____	
Date Moderated: _____	Moderator Signature: _____	

**Simulation 4A: J-K flip-flop circuit****4.4.1 Purpose:**

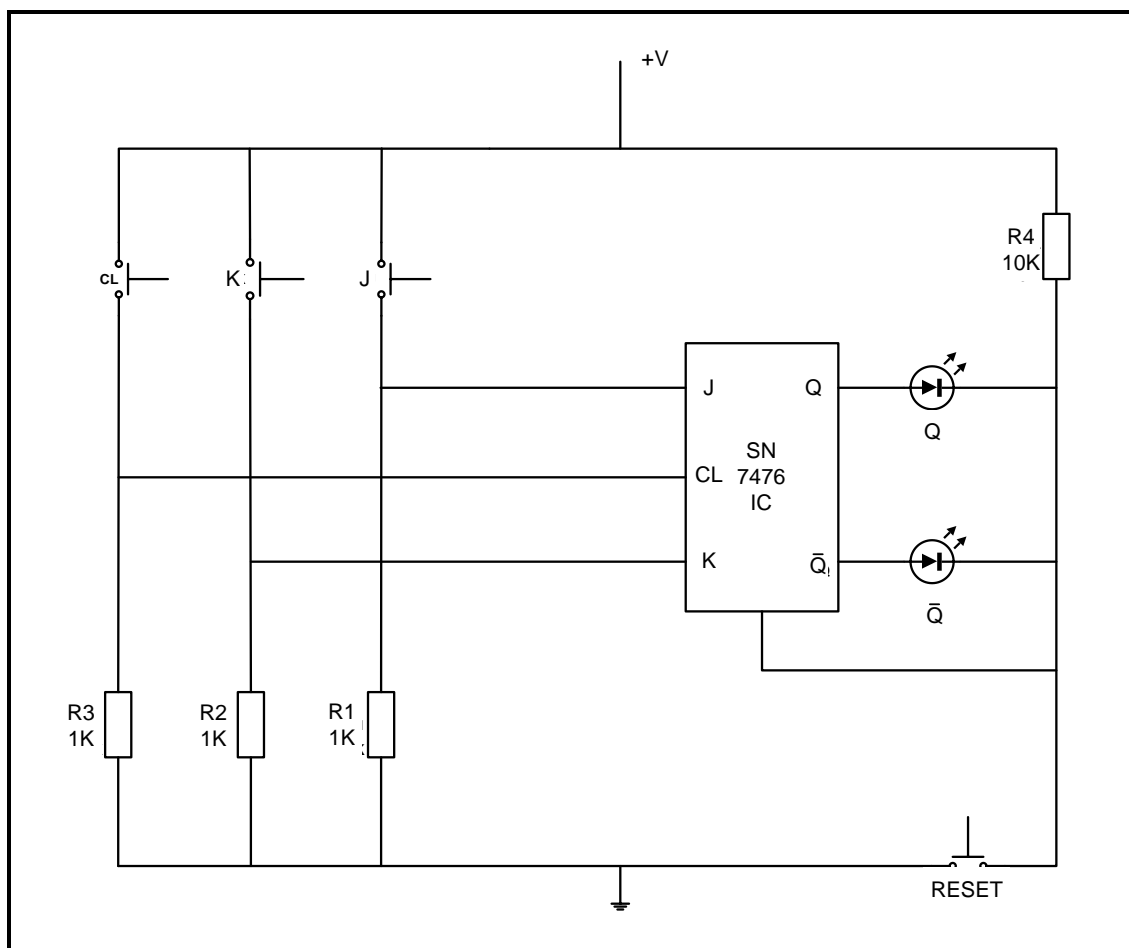
- To demonstrate the operation of the J-K latching practically

**4.4.2 Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Breadboard	SN7476 IC
Voltmeter	Toggle switches x 4
Dual power supply 9 V 0–9 V	1 kΩ resistor x 3
Dual power supply 5 V 0–5 V	10 kΩ resistor x 1
Side cutters	1 x red and 1 x green LED
Wire stripper	Connecting wires

### 4.4.3 Circuit diagram

Connect the circuit as in FIGURE 4.3.3 on the breadboard. After you switch on the circuit, press the reset switch. You will be assessed with the rubric that follows.



**FIGURE 4.3.3: CIRCUIT DIAGRAM OF A J-K FLIP-FLOP**

### 4.4.4 Procedure:

- Apply logic 0 to J and K input and 1 to the CL, and observe the  $Q$  and  $\bar{Q}$  output.
- Apply logic 0 to J and logic 1 to K input and 1 to the CL, and observe the  $Q$  and  $\bar{Q}$  output.
- Apply logic 1 to J and logic 0 to K input and 1 to the CL, and observe the  $Q$  and  $\bar{Q}$  output.
- Apply logic 1 to J and logic 1 to K input and 1 to the CL, and observe the  $Q$  and  $\bar{Q}$  output.

### 4.4.5 Observations:

- (a) Press the J and K switches. Write down your observation.

\_\_\_\_\_ (1)

- (b) Press the clock and J switches simultaneously. Write down your observation.

\_\_\_\_\_ (1)

4.4.6 Complete the truth table based on the operation of the circuit you have constructed.

INPUTS			OUTPUTS	
$J$	$K$	$CL$	$Q$	$\overline{Q}$
0	0	0		
0	1	0		
1	0	0		
1	1	0		
0	0	1		
0	1	1		
1	0	1		
1	1	1		

(8)

#### 4.4.7 Housekeeping

When you have obtained all the measurements and the teacher has validated all your answers, you must tidy up your workplace as part of the safety in the workshop. You will be assessed on housekeeping with the rubric below.

## FACET SHEET FOR SIMULATION 4A

Task description	Mark allocation (tick the appropriate level next to the task indicated)				Allocation of marks
	Competent after reassessment of certain parts of the task	Not yet competent after reassessment of certain/all parts of the task	Competent	Outstanding (Highly competent)	
<b>Building the J-K flip-flop circuit</b>	The learner was given opportunities to rebuild the circuit after the teacher intervened in identifying and rectifying more mistakes. <b>(1)</b>	The learner was given an opportunity to rebuild part of the circuit after the teacher intervened in identifying and rectifying a few mistakes. <b>(2–3)</b>	The learner correctly built the circuit without the guidance of the teacher. <b>(4–5)</b>	The learner correctly built the circuit without the guidance of the teacher and went beyond expectations and with high proficiency. <b>(6–9)</b>	<u>9</u>
<b>Safety aspects</b>	The learner was timeously reminded to apply safety rules, regulation and correct procedure when using tools and instruments. <b>(1)</b>	The learner was sometimes reminded to apply safety rules, regulation and correct procedure when using tools and instruments. <b>(2)</b>	The learner applied safety rules, regulation and correct procedure when using tools and instruments to wire the circuits without being reminded by the teacher. <b>(3)</b>		<u>3</u>
<b>Attitude/ Behaviour/ Conduct</b>	The learner was reluctant to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice even after being cautioned/reprimanded. <b>(0)</b>	The learner was reluctant to a certain degree to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. <b>(1–2)</b>	The learner demonstrated willingness to work, cooperate, take responsibility of their own conduct and follow instructional, regulation and workshop practice. <b>(3)</b>		<u>3</u>
<b>Rubric Theory</b> <b>Total Simulation 4A</b>					/15 + /10 = /25

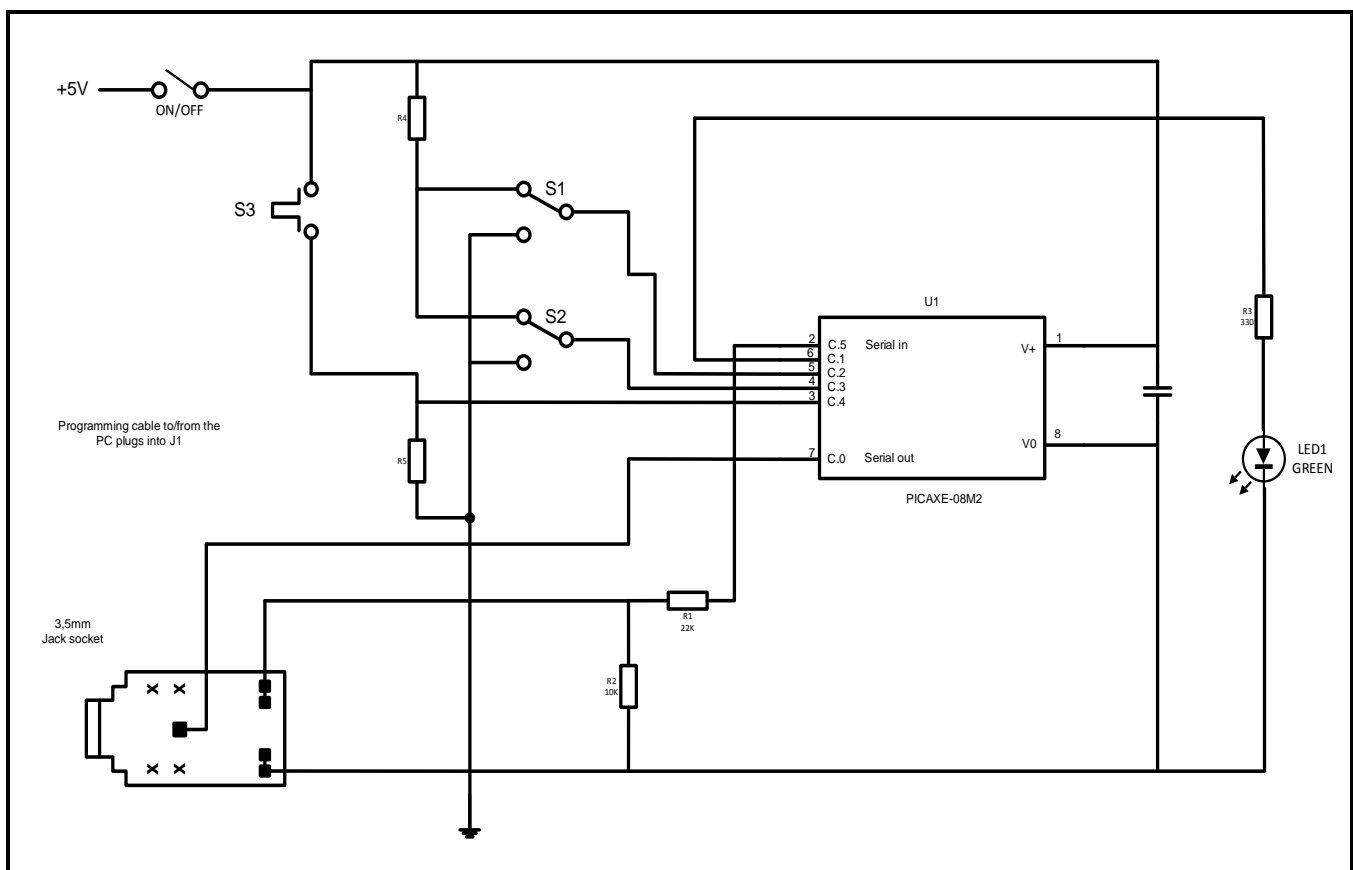
**Simulation 4B: PICAXE****4.4.8 Purpose:**

- To test knowledge of flow diagrams and PICAXE

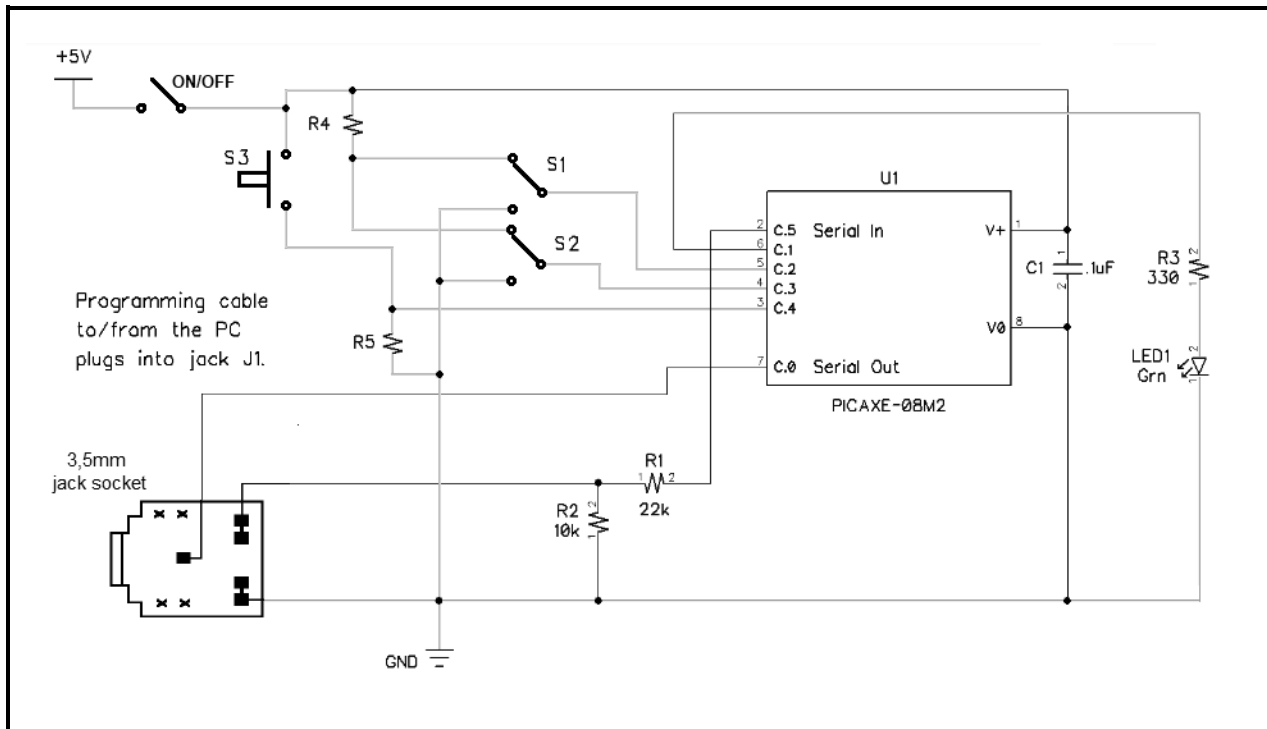
Study the PICAXE circuit below and design a flow diagram for the circuit.

**SCENARIO:**

To start the program, S3 should be activated. The LED will be ON when either S1 or S2 is activated. If S1 is activated, the LED will be ON for 2 seconds and once the preset time has lapsed, the program will start again from the beginning. If S2 is activated, the LED will be ON for 5 seconds and once the preset time has lapsed, the program will start again from the beginning. This process should continue indefinitely.








STEP	PROGRAM LINES	MARK ALLOCATION
1.	Program lines to activate/de-activate switch 1	3
2.	Program lines to activate/de-activate switch 1	3
3.	Program lines to activate/de-activate switch 1	3
4.	Program line to switch LED ON for 2 s	2
5.	Program line to switch LED OFF	1
6.	Program line to switch LED ON for 5 s	2
7.	Program line to switch LED OFF	1
	<b>TOTAL</b>	<b>15</b>

## FACET SHEET FOR SIMULATION 4B

Task description	Mark allocation (tick the appropriate level next to the task indicated)				Allocation of marks
	Competent after reassessment of certain parts of the task	Not yet competent after reassessment of certain/all parts of the task	Competent	Outstanding (Highly competent)	
Inserting the Start/Stop element			Start element correctly placed (1)	Stop element correctly placed (2)	$\frac{2}{2}$
Inserting the decision element			One decision element correctly placed (1)	Two decision elements correctly placed (2)	$\frac{2}{2}$
Inserting the process element	No process element correctly placed (0)		One process element correctly placed (1)		$\frac{1}{1}$
Inserting the data elements	One data element correctly placed (1)	Two data elements correctly placed (2)	Three data elements correctly placed (3)	Five data elements correctly placed (4–5)	$\frac{5}{5}$
Inserting the flow lines correctly	0%–25% of flow lines correctly placed (0–2)	25%–50% of flow lines correctly placed (3–4)	50%–75% of flow lines correctly placed (5–6)	All flow lines correctly placed (9)	$\frac{9}{9}$
Labelling of elements	0–3 labels correctly placed (0–1)	4–6 labels correctly placed (2–3)	7–9 labels correctly placed (4–5)	All labels correctly placed (6)	$\frac{6}{6}$
<b>Rubric</b> <b>Total Simulation 4A</b> <b>Total Simulation 4B</b> <b>TOTAL:</b>					 = /25 + /25 = /50

**5. SECTION B: DESIGN AND MAKE**

<b>Design and Make Project</b>		
Time: January to August 2023		
Learner Name:		
School:		
Class:		
Title/Type of Project: _____		

**INSTRUCTIONS**

- This section is **COMPULSORY** for all learners.
- The teacher will choose a circuit for the project.
- Any project constructed must include at least (but is not limited to):
  - Seven components
  - A variety of components (both active and passive)
  - PCB making in some form
  - Soldering
  - An enclosure with a switch and protection
- The checklist below must be used to ensure that all the required tasks for the PAT have been completed.

**PAT CHECKLIST**

The learner **MUST** fill in this checklist **BEFORE** marking of the section takes place.

NO.	DESCRIPTION	TICK (☑)	
		NO	YES
Design and Make: Part 1			
1.	Circuit diagram drawn	<input type="checkbox"/>	<input type="checkbox"/>
2.	Circuit description filled in	<input type="checkbox"/>	<input type="checkbox"/>
3.	Component list completed	<input type="checkbox"/>	<input type="checkbox"/>
4.	Tools list for circuitry populated	<input type="checkbox"/>	<input type="checkbox"/>
5.	Measuring instrument list filled in	<input type="checkbox"/>	<input type="checkbox"/>
Design and Make: Part 2			
1.	Enclosure design completed and included in the file	<input type="checkbox"/>	<input type="checkbox"/>
2.	Unique name written down and on the enclosure	<input type="checkbox"/>	<input type="checkbox"/>
3.	Logo designed and on the enclosure	<input type="checkbox"/>	<input type="checkbox"/>
Miscellaneous			
1.	Enclosure included in the project	<input type="checkbox"/>	<input type="checkbox"/>
2.	Enclosure prepared and drilled according to the design	<input type="checkbox"/>	<input type="checkbox"/>
3.	Enclosure finished off and completed with name and logo	<input type="checkbox"/>	<input type="checkbox"/>
4.	PCB securely mounted in the enclosure using acceptable techniques	<input type="checkbox"/>	<input type="checkbox"/>
5.	Circuit inside the enclosure accessible	<input type="checkbox"/>	<input type="checkbox"/>
6.	Internal wiring neat and ready for inspection	<input type="checkbox"/>	<input type="checkbox"/>
7.	File and project completed and ready for moderation at the workshop/room	<input type="checkbox"/>	<input type="checkbox"/>

## 5.1 Design and Make: Part 1

### 5.1.1 Circuit diagram

Draw a circuit diagram of the project chosen and paste it on the next page.

### 5.1.2 Project: Description of operation

Use the space below to describe how the project operates. Do research and use your own words.

This image shows a full page of blank, lined paper. It features approximately 20 evenly spaced horizontal black lines running across the width of the page, typical of notebook or composition paper. The lines are uniform in thickness and spacing, providing a guide for handwriting. There are no margins, text, or other markings on the page.



**5.2 Assessment of the Design and Make Phase: Part 1**

NO.	FACET DESCRIPTION	Mark	Achieved mark
<b>Circuit Diagram</b>			
1.	The circuit diagram was drawn using <ul style="list-style-type: none"> <li>EGD equipment (4)</li> <li>CAD/Any electronic design software (6)</li> </ul>	6	
2.	The circuit diagram was drawn using correct symbols.	3	
3.	The circuit diagram has all labels, e.g. R1, C1, Tr1	3	
4.	The circuit diagram has all component values, e.g. 100 $\Omega$ , 220 $\mu\text{F}$	4	
5.	The circuit diagram has a name/title.	2	
6.	The circuit diagram has a frame and title block.	2	
	<b>Circuit Diagram Subtotal:</b>	<b>20</b>	
<b>Component List</b>			
7.	Labels correlate with circuit diagram.	2	
8.	Description and values correlate with circuit diagram.	2	
9.	Quantities are correct.	1	
	<b>Component List Subtotal:</b>	<b>5</b>	
<b>Description of Operation</b>			
10.	Basic function of the circuit is described correctly. The purpose/role/function of each component is described.	11	
11.	All subcircuits in the circuit diagram and component list are included in the description.	4	
12.	Purposes of subcircuits in the circuit diagram are described correctly.	5	
13.	Learner used own interpretation and did not copy from another source verbatim.	3	
14.	Sources are acknowledged.	2	
	<b>Description of Operation Subtotal:</b>	<b>25</b>	
<b>Tools/Instrument List</b>			
15.	The tools/instrument list has been completed.	4	
16.	The tools/instruments listed all have a purpose for being used.	1	
	<b>Tools/Instrument List Subtotal:</b>	<b>5</b>	

NO.	FACET DESCRIPTION	Mark	Achieved mark
<b>Circuit Board Manufacturing</b>			
17.	Transfer of the PCB design onto the blank board is correct. Not over-exposed or under-exposed.	5	
18.	Circuit board is etched neatly according to the PCB design.	10	
19.	The learner's name is etched onto the circuit design.	4	
20.	All burrs are removed.	2	
21.	Axial and radial components are placed neatly and flush with the board.	5	
22.	Component orientation are aligned between similar components (e.g. the gold band of all resistors are placed on the same side).	2	
23.	Soldered components – leads are cut off, flush and neat on the solder side.	5	
24.	More than 60% of the solder joints are shiny (not dry joints).	5	
25.	Wire insulation is stripped to the correct length (no extra copper showing).	3	
26.	Wiring is long enough to allow for dismantling and inspection.	2	
27.	Wiring is wrapped neatly.	2	
28.	A power switch is included and fitted to the enclosure.	2	
29.	A fuse/protection is included and fitted correctly where applicable.	2	
30.	Wiring entering/exiting the enclosure is provided with a grommet/applicable fittings/sockets where applicable.	2	
31.	Batteries/Transformer is mounted using a battery housing/mounting bracket and battery clip (NO double-sided tape).	2	
32.	The project has a pilot light/LED installed in the enclosure showing when the circuit is operational. LED is mounted with a grommet or applicable fitting. (Switch is on – must go out when fuse is blown.)	2	
33.	The project is fully operational and commissioned/installed in the enclosure.	10	
	<b>Circuit Board Manufacturing Subtotal:</b>	<b>65</b>	
	<b>Circuit Diagram Subtotal:</b>	<b>20</b>	
	<b>Component List Subtotal:</b>	<b>5</b>	
	<b>Description of Operation Subtotal:</b>	<b>25</b>	
	<b>Tools/Instrument List Subtotal:</b>	<b>5</b>	
	<b>Circuit Board Manufacturing Subtotal:</b>	<b>65</b>	

<b>TOTAL</b> <b>(PART 1 = 120 marks)</b>	
---	--

<b>NOTE:</b> In projects where facets are not applicable, the projects should be marked and the totals adjusted accordingly.
--

**5.3 Design and Make: Part 2****5.3.1 Enclosure design**

- Design an enclosure for your project.
- NO FREEHAND DRAWINGS.
- Draw using EGD equipment **OR** use a CAD program.
- Draw in first-angle orthographic projection.
- Add your drawings after this page.
- Use colour to enhance your drawing.

**5.3.2 Manufacture the enclosure neatly according to your design.**

You may use pre-cut panels from metal, wood and/or Perspex/Plexiglas.

You must, however, construct/assemble these parts.

Injection moulded enclosures are also acceptable. It is important that your enclosure and the placement of the parts align with your design.

**5.3.3 Choose a name for your device.**

Write down the name of the device below.

---

**5.3.4 Design a unique logo for your device, as well as a specification plate and attach it after this page.**



**5.4 Assessment of the Design and Make Phase: Part 2**

NO.	FACET DESCRIPTION	Mark	Achieved mark
<b>Enclosure Design</b>			
1.	Enclosure design is included in first-angle orthographic projection.	2	
2.	Drawn design includes a title box and page border.	1	
3.	Isometric drawing included additionally.	2	
4.	Dimensions are included.	2	
5.	The name of the device is written in the PAT document.	1	
6.	The logo design and specification plate design is in the PAT document.	2	
	<b>Enclosure Design Subtotal:</b>	<b>10</b>	
<b>Enclosure Manufacturing</b>			
7.	Enclosure matches the design. Dimensions and placement correlate.	1	
8.	Name of the device is attached on the enclosure.	1	
9.	The logo design is attached on the enclosure.	2	
10.	The logo design on the enclosure is durable and not merely a paper pasted on the enclosure (painted/used decoupage/screen printed/sublimation printed).	2	
11.	The enclosure is manufactured from scratch/pre-cut parts.  Does NOT include: cardboard, paper, margarine container Does include: sheet metal, Perspex, Plexiglas, wood, glass and other raw materials, injection-moulded plastic boxes	5	
12.	Holes/Cut-outs in the enclosure are made with the appropriate tools.	3	
13.	Specification plate with the learner's name, operating voltage, fuse rating and additional information on the project.	2	
14.	Enclosure is neatly prepared, painted and aesthetically pleasing.	2	
15.	The circuit board is mounted using appropriate methods inside the enclosure. (NO double-sided tape, Prestik, glue, chewing gum, masking tape, etc.)	2	
	<b>Enclosure Manufacturing Subtotal:</b>	<b>20</b>	

<b>TOTAL</b> <b>(PART 2 = 30 marks)</b>	
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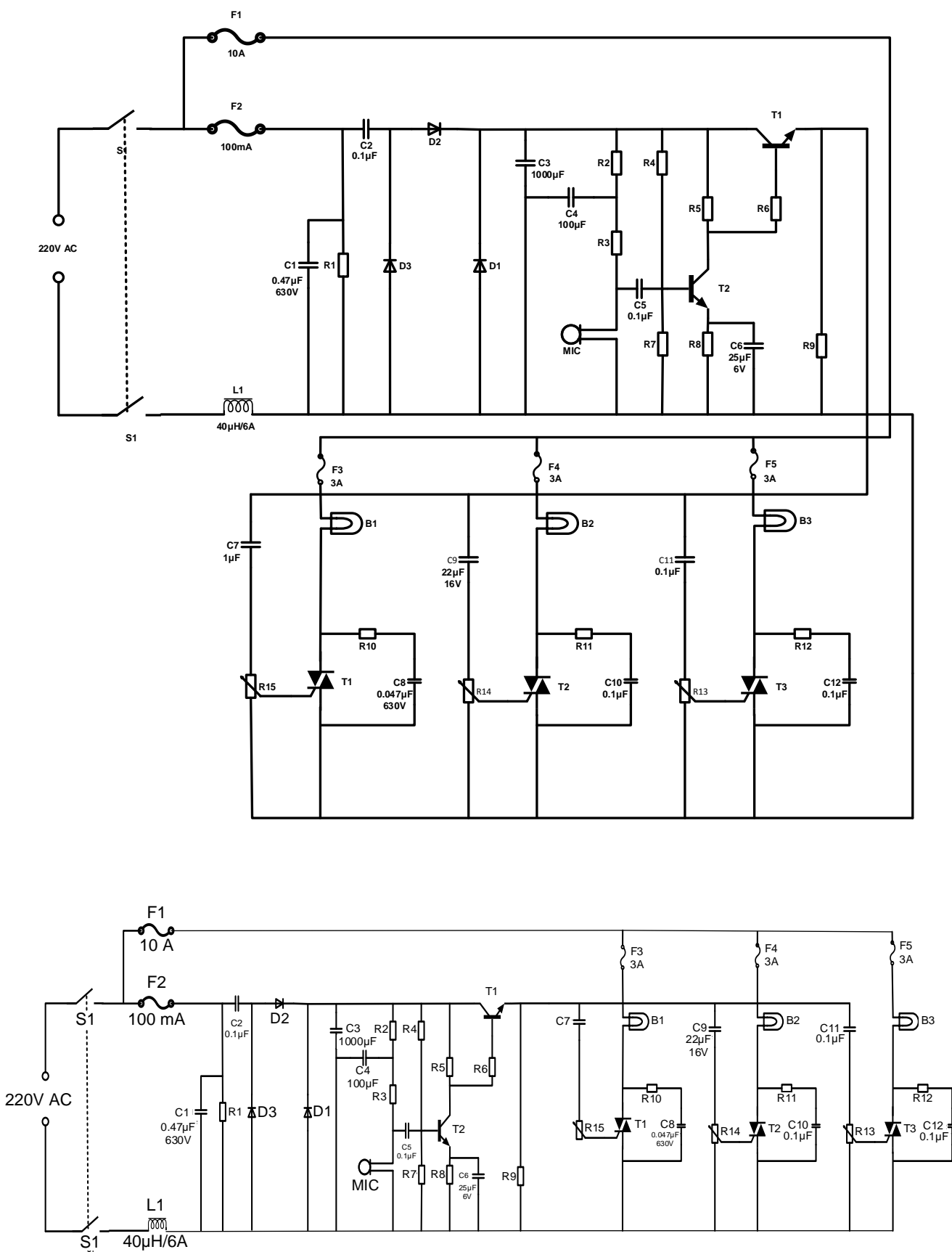
## 6. PROJECTS

### 6.1 Practical Project 6.1: Sound-to-light Controller

This sound-controlled light circuit design is used to control the brightness of the lights attached to it in sync with the sound that is being captured by its microphone. This electronic circuit design is very common in disco houses, bars, parties, etc.

Usually, sound-controlled lights are just connected in parallel with the loudspeakers. This configuration has two disadvantages: a very power amplifier can destroy the lights, or worse, a defective light can destroy the amp. This problem is avoided by the circuit by not connecting directly to the amp. Instead, it picks up the sound with its microphone.

The power-supply part is on the left of the electret microphone amplifier and the light controller part is on the right. The capacitors C2 and C3 are the capacitive voltage divider and reduces the power supply level. Diodes D1 and D2 rectify the positive swing of the AC voltage. The network composed of L1 and C1 protects the power line from voltage surges. In this circuit design, an electret microphone is being used. Take note that there are two types of electret mics. The first type has three pins for power, ground and output. The second type has only two pins. The second type is used for this circuit.

**SOUND-TO-LIGHT CONTROLLER CIRCUIT**

COMPONENT LIST	
R1 = 560 k $\Omega$ /1 W	C8, C12 = 0,047 $\mu$ F/630V
R2, R3 = 15 k $\Omega$ ¼ W	C9 = 22 $\mu$ F 16 V
R4 = 33 k $\Omega$ /¼ W	C11 = 47 $\mu$ F 16 V
R5, R6, R9 = 1 k $\Omega$ ¼ W	D1, D2 = 1N4004
R7 = 18 k $\Omega$ ¼ W	D3 = 1N4742 12v/1 W
R8 = 560 $\Omega$ ¼ W	F1 10 A fuse 220 V
R10, R11, R12 = 100 k $\Omega$	F2 100 mA fuse 220 V
P1, P2, P3 = 5 k $\Omega$ Pot	F3, F4, F5 220 V 3 A fuse
C1 = 0,47 $\mu$ F 630 V	L1 = 40 $\mu$ H 6 A
C2, C5 0,1 $\mu$ F/220 V	B1, B2, B3 = 60 W incandescent lamp
C3 1 000 $\mu$ F/16 V	Mic = low-impedance microphone
C4 100 $\mu$ F/16 V	
C6 25 $\mu$ F/6 V	
C7 1 $\mu$ F 16 V	

**WARNING:**

Some parts in the circuit board are subject to lethal potential because the device is connected to 230 V AC. When plugging in the project, place it in a plastic or wooden box to prevent the circuit from shocking you. Avoid connecting this circuit to other appliances (e.g. to the output of an amplifier by means of a cable) because of the absence of a mains transformer. Use only the microphone in the main case to pick up the sound.

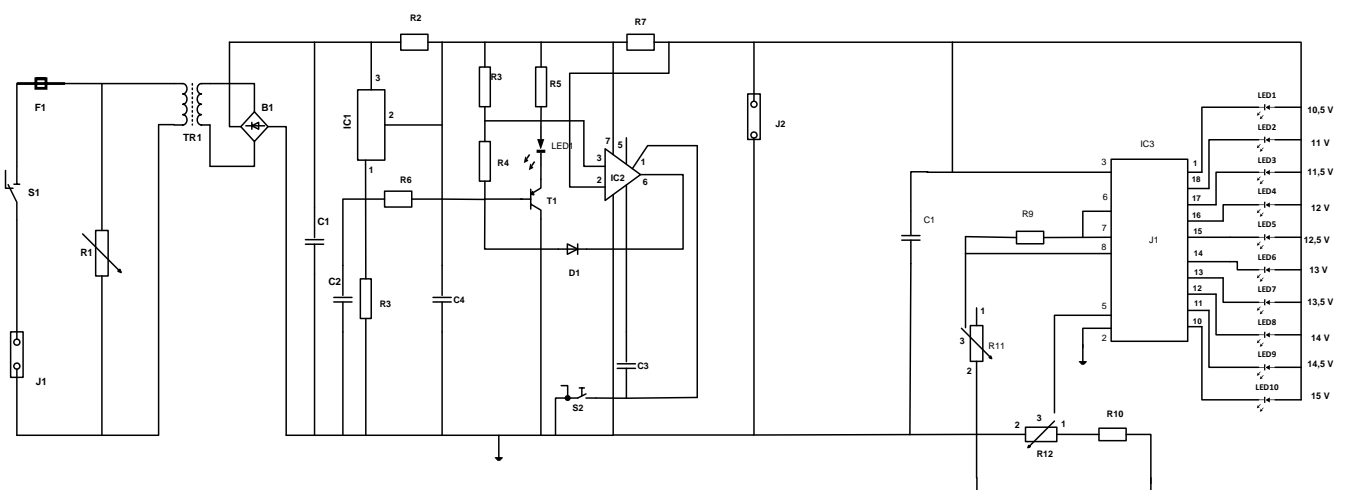
## 6.2 Practical Project 6.2: Automatic Battery Charger with Battery-voltage Bar-graph Display

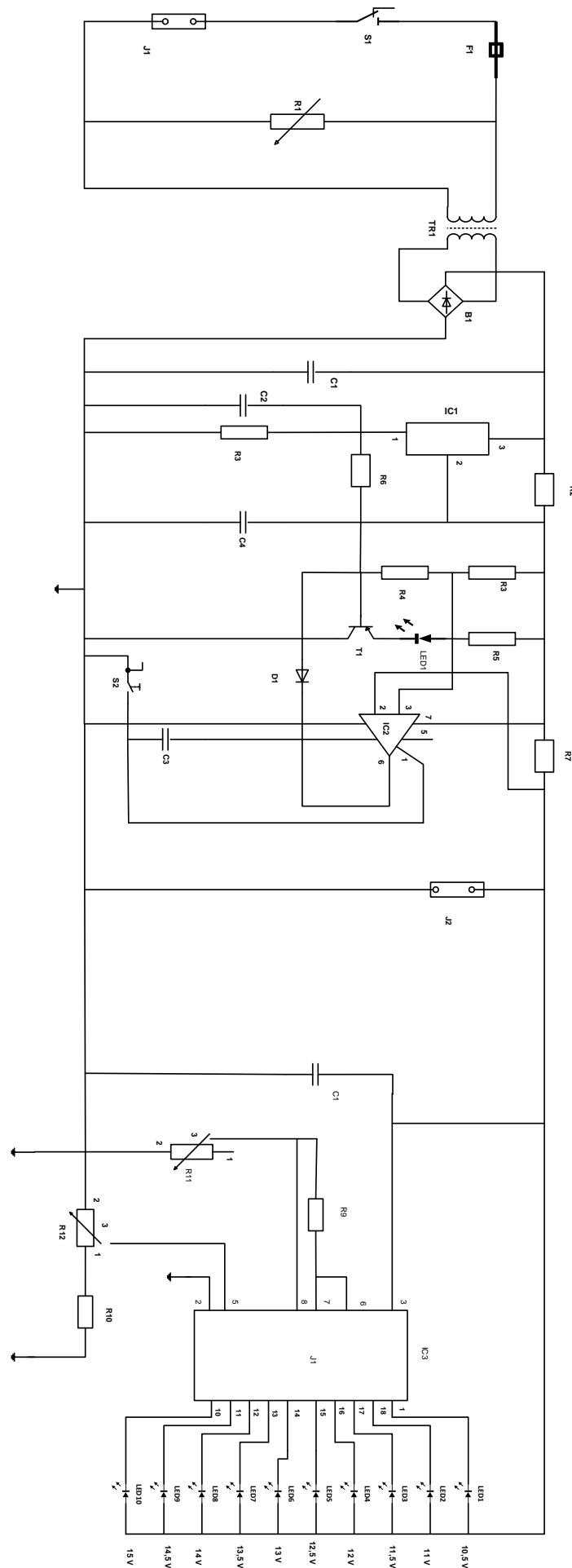
This automatic battery charger project is based on the National Semiconductor LM350 3 A adjustable regulator. It is designed to charge 12 V lead-acid batteries. When the switch SW1 is pushed, the output of the charger will go up to 14,5 V. The initial charging current is limited to 2 A. As the charge of the battery continues to rise, the charging current decreases to 150 mA and the output voltage is reduced to 12,5 V. At this stage the charging is terminated and the light-emitting diode lights up to indicate that the charging process has been completed.

The schematic diagram below shows how the various components are connected. The first part of the diagram shows how the DC power supply to LM350 is achieved. The combined use of varistor V1 and fuse F1 is to protect the circuit from overcurrent and power surge of the mains supply.

Transformer T1 is used to step down the input voltage from the mains to 16 V AC. Diode bridge DB and electrolytic capacitor E1 are used to rectify the AC voltage to DC voltage. This rectified DC power supply is fed into the input of the second circuit where LM350 and operational amplifier LM301A are used to control the charging current and voltage of the lead-acid battery. Once the charge is full, transistor Q1 will turn ON and LED L1 will be ON to indicate that the charging has been completed. A heat sink is attached to LM350 to transfer the heat generated from the regulator to the ambient.

This bar-graph LED-battery-level-indicator project is based on the LM3914 monolithic IC of the National Semiconductor that senses the voltage levels of the battery and drives the 10 light-emitting diodes based on the voltage level that is detected. It provides a linear analogue display output and has a pin that can be configured to display the output in moving dot or bar graph. The current driving the LEDs is regulated and programmable, hence limiting resistors are not required. The schematic diagram below shows how the various components are connected. Switch S1 is used to change the display type from moving dot to bar graph type. When S1 is ON, the display type is bar graph, but when it is OFF, the display changes to the moving dot type. R3 is used to set the lower limit of the display. Use a variable DC power supply and set the VBAT to 10,5 V. Adjust VR1 until the LED L1 turns ON. Next, set the VBAT to 15 V; adjust VR2 until all the LEDs turn ON (when S1 is ON).





COMPONENT LIST	
R1 varistor 14 mm	B1 5 A diode bridge
R2 500 ohm, 5 W	C1 6 800 uF 35 V electrolytic capacitor
R3, R6 15 K ¼ W	C2 0,1 uF ceramic 104
R4 230 ohm ¼ W	C3 1 nF ceramic 102
R5 1k	C4 1 uF electrolytic 25 volt
R7 0,2 ohm, 5 W	D1 1N 4148 diode
R8 3k3 ¼ W	IC1 LM350 16 volt positive voltage regulator
J1 mains supply	IC2 LM301 H operational amplifier
J2 12 V connector for battery/battery clamps	S1 On/Off switch for mains voltage
F1 500 mA fast-blow fuse	S2 push-to-make switch
TR1 240 V–16 V transformer 3 A (+/-50 VA)	LED 1 red LED 5 mm
R9 1k2 ¼ W 5%	IC 3 LM3914 N bar-graph display driver
R10 4k7 ¼ W 5%	C1 10 µF 25 volt electrolytic capacitor
R11 5k potentiometer	S1 SPST toggle switch
LED 1–10 LED – red, amber, green	
R12 5k potentiometer	

## 7. CONCLUSION

On completion of the practical assessment task, learners should be able to demonstrate their understanding of the industry, enhance their knowledge, skills, values and reasoning abilities as well as establish connections to life outside the classroom and address real-world challenges. The PAT furthermore develops learners' life skills and provides opportunities for learners to engage in their own learning.